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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,244	08/18/2003	Sheng-Chih Lai	0941-0809P	8162

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
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2823

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Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Examiner's Answer-No option to Reopen Prosecution

1. Responsive to Applicants Reply Brief filed on May 16, 2006, a supplemental Examiner's Answer is set forth below: Applicants contend that Johnson, U.S. Patent 6,525,953 B1 fails to disclose diodes because anti-fuse material located between the diode components. Applicants further state that there is no diode until the anti-fuse layer becomes conductive, so therefore in one state there is no diode and in another state there is a diode and no dielectric in the other state. Furthermore, the language of the claim is that the dielectric layers are "on the diodes".

In response to Applicants contention that Johnson fails to disclose a diode, Applicants are directed to column 5, lines 15-25 and column 8, lines 45-48 which has support for **FIGS. 4-6** for a pre-existing Schottky diode (which is element ii in column 5 line 18) as well as the diodes with a state change element such as an anti-fuse layer (see column 1, lines 19-24). It is well known that a Schottky diode is formed from a metal-semiconductor junction. Support for the Schottky diode can be found not only in **FIGS. 4-6**, but also in column 8, lines 45-48 where conductive layers **114** and **123** includes elemental metals such as aluminum. It is well known that aluminum is in the group III category of the periodic table, which is considered p-type material. **FIGS. 4-6** discloses a heavily doped n⁺ layer next to conductive material 114/123. Because an n-type material is adjoined to a p-type material (i.e., aluminum) a Schottky diode is inherently formed.

With respect to the dielectric/insulator being formed on the diodes Johnson clearly discloses that each pillar is isolated from neighboring pillars by a pair of self-aligned etch steps and subsequent dielectric depositions (column 1, lines 24-26). Furthermore it is well known to passivate

Art Unit: 2823

semiconductor devices with a dielectric to further enhance electrical connections to the devices, this passivation process inherently is on top and surrounding the semiconductor device.

Appellant may file another reply brief in compliance with 37 CFR 41.41 within two months of the date of mailing of this supplemental examiner's answer. Extensions of time under 37 CFR 1.136(a) are not applicable to this two month time period. See 37 CFR 41.43(b)-(c).

A Technology Center Director or designee has approved this supplemental examiner's answer by signing below:



W. DAVID COLEMAN
PRIMARY EXAMINER



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800



RICKY MACK
SUPERVISORY PATENT EXAMINER